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Jameco Part Number 198619

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS240 • DM74LS241
Octal 3-STATE Buffer/Line Driver/Line Receiver

General Description

These buffers/line drivers are designed to improve both the performance and PC board density of 3-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

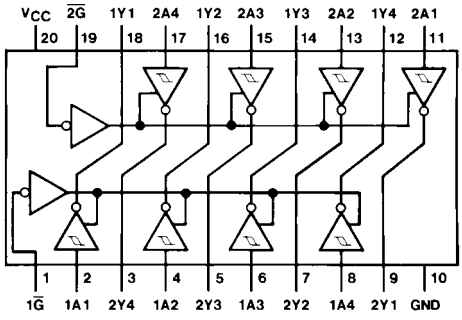
- 3-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at data inputs improves noise margins
- Typical I_{OL} (sink current)
  24 mA
- Typical I_{OH} (source current)
  −15 mA
- Typical propagation delay times
  Inverting 10.5 ns
  Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
  Inverting 130 mW
  Noninverting 135 mW

Ordering Code:

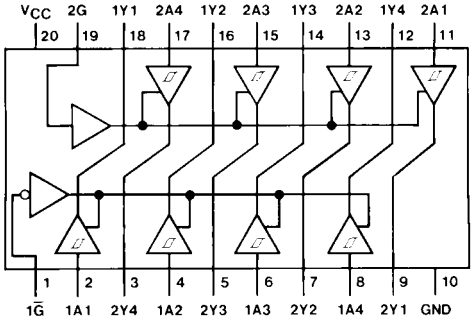
Order Number	Package Number	Package Description
DM74LS240WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS240N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74LS241WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS241N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams



DM74LS240



DM74LS241

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Function Tables

DM74LS240

Inputs		Output
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Z

DM74LS241

Inputs				Outputs	
G	$\overline{G}$	1A	2A	1Y	2Y
X	L	L	X	L	
X	L	H	X	H	
X	H	X	X	Z	
H	X	X	L		L
H	X	X	H		H
L	X	X	X		Z

L = LOW Logic Level
H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
Z = High Impedance

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−15	mA
I_{OL}	LOW Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$) Data Inputs Only	V_{CC} = Min		0.2	0.4		V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1 mA		2.7			V
		V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −3 mA		2.4	3.4		
		V_{CC} = Min, V_{IH} = Min V_{IL} = 0.5V, I_{OH} = Max		2			
V_{OL}	LOW Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	I_{OL} = 12 mA			0.4	V
			I_{OL} = Max			0.5	
I_{OZH}	Off-State Output Current, HIGH Level Voltage Applied	V_{CC} = Max V_{IL} = Max V_{IH} = Min	V_O = 2.7V			20	µA
I_{OZL}	Off-State Output Current, LOW Level Voltage Applied		V_O = 0.4V			−20	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max V_I = 7V				0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)		−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs OPEN	Outputs HIGH		13	23	mA
			Outputs LOW		26	44	
					27	46	
			Outputs Disabled		29	50	
					32	54	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

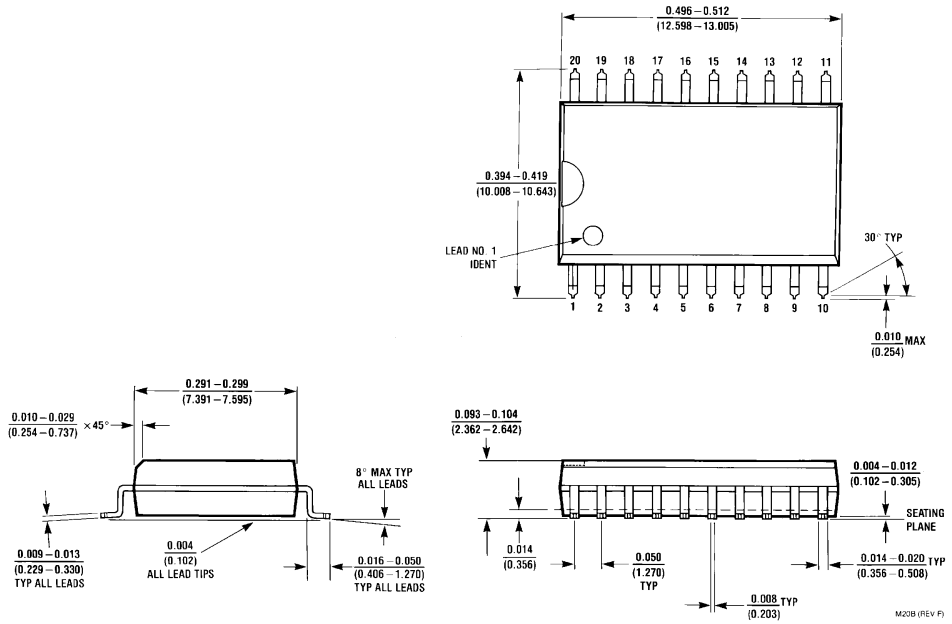
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

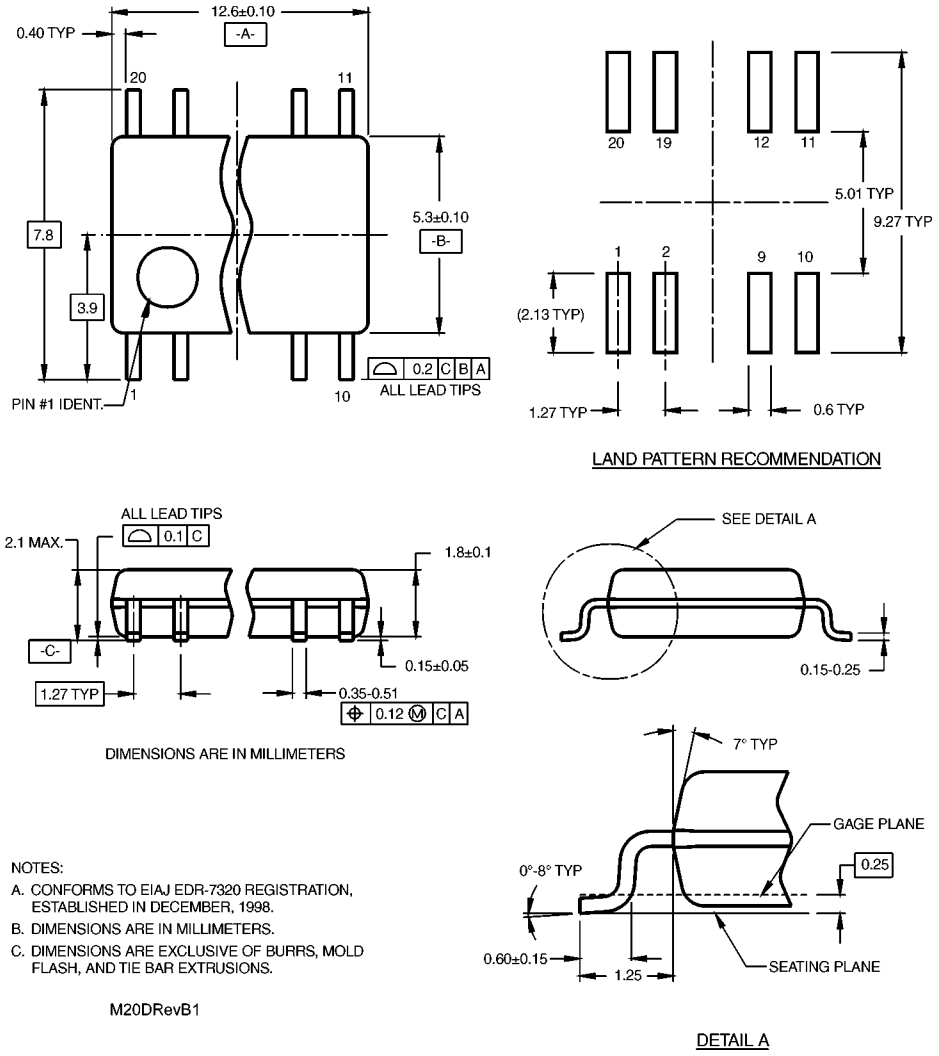
Symbol	Parameter	Conditions		Max	Units
t_{PLH}	Propagation Delay Time	C_L = 45 pF	DM74LS240	14	ns
	LOW-to-HIGH Level Output	R_L = 667Ω	DM74LS241	18	
t_{PHL}	Propagation Delay Time	C_L = 45 pF	DM74LS240	18	ns
	HIGH-to-LOW Level Output	R_L = 667Ω	DM74LS241	18	
t_{PZL}	Output Enable Time	C_L = 45 pF	DM74LS240	30	ns
	to LOW Level	R_L = 667Ω	DM74LS241	30	
t_{PZH}	Output Enable Time	C_L = 45 pF	DM74LS240	23	ns
	to HIGH Level	R_L = 667Ω	DM74LS241	23	
t_{PLZ}	Output Disable Time	C_L = 5 pF	DM74LS240	25	ns
	from LOW Level	R_L = 667Ω	DM74LS241	25	
t_{PHZ}	Output Disable Time	C_L = 5 pF	DM74LS240	18	ns
	from HIGH Level	R_L = 667Ω	DM74LS241	18	
t_{PLH}	Propagation Delay Time	C_L = 150 pF	DM74LS240	18	ns
	LOW-to-HIGH Level Output	R_L = 667Ω	DM74LS241	21	
t_{PHL}	Propagation Delay Time	C_L = 150 pF	DM74LS240	22	ns
	HIGH-to-LOW Level Output	R_L = 667Ω	DM74LS241	22	
t_{PZL}	Output Enable Time	C_L = 150 pF	DM74LS240	33	ns
	to LOW Level	R_L = 667Ω	DM74LS241	33	
t_{PZH}	Output Enable Time	C_L = 150 pF	DM74LS240	26	ns
	to HIGH Level	R_L = 667Ω	DM74LS241	26	

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

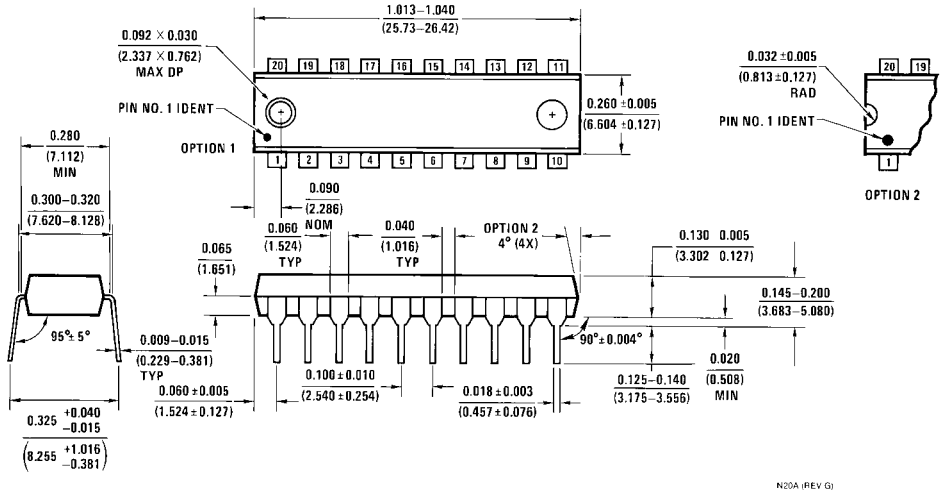
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Description M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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